

P0001

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* W E L C O M E T O T H E
* U . S . P A T E N T T E X T F I L E
* * * * *

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L1      24220 395/?/CCLS

=> s l1 and (superscalar or (rename (w) register?))
      345 SUPERSCALAR
      473 RENAME
      191196 REGISTER?
      15 RENAME (W) REGISTER?
L2      267 L1 AND (SUPERSCALAR OR (RENAME (W) REGISTER?))

=> s l1 and (superscalar? or (rename (w) register?))/ab
      57 SUPERSCALAR?/AB
      20 RENAME/AB
      20922 REGISTER?/AB
      2 RENAME (W) REGISTER?
L3      53 L1 AND (SUPERSCALAR? OR (RENAME (W) REGISTER?))/AB

=> s l1 and ((reservation (w) station?) or (out (3w) sequence (3w) execut?))/ab
      262 RESERVATION/AB
      59584 STATION?/AB
      14 RESERVATION (W) STATION?
      123370 OUT/AB
      26465 SEQUENCE/AB
      11691 EXECUT?/AB
      2 OUT (3W) SEQUENCE (3W) EXECUT?
L4      15 L1 AND ((RESERVATION (W) STATION?) OR (OUT (3W) SEQUENCE (3W)
      EXECUT?))/AB
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L1      24220 S 395/?/CCLS
L2      267 S L1 AND (SUPERSCALAR OR (RENAME (W) REGISTER?))
L3      53 S L1 AND (SUPERSCALAR? OR (RENAME (W) REGISTER?))/AB
L4      15 S L1 AND ((RESERVATION (W) STATION?) OR (OUT (3W) SEQUENCE (3
```

=> s l4 or l4

```
L5      15 L4 OR L4
```

=> s l3 or l4

```
L6      64 L3 OR L4
```

=> s l6 and (multiplexer?)

38300 MULTIPLEXER?

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L7      38 L6 AND (MULTIPLEXER?)
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=> d his

(FILE 'USPAT' ENTERED AT 10:37:01 ON 28 JAN 1998)

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L1      24220 S 395/?/CCLS
L2      267 S L1 AND (SUPERSCALAR OR (RENAME (W) REGISTER?))
L3      53 S L1 AND (SUPERSCALAR? OR (RENAME (W) REGISTER?))/AB
L4      15 S L1 AND ((RESERVATION (W) STATION?) OR (OUT (3W) SEQUENCE (3
L5      15 S L4 OR L4
L6      64 S L3 OR L4
L7      38 S L6 AND (MULTIPLEXER?)
```

=> d l7 1-38

1. 5,706,491, Jan. 6, 1998, Branch processing unit with a return stack including repair using pointers from different pipe stages; Steven C. McMahan, 395/581, 569, 585, 586 [IMAGE AVAILABLE]
2. 5,689,720, Nov. 18, 1997, High-performance superscalar-based computer system with out-of-order instruction execution; Le Trong Nguyen, et al., 395/376, 382, 383, 391, 569, 571, 582 [IMAGE AVAILABLE]
3. 5,689,674, Nov. 18, 1997, Method and apparatus for binding instructions to dispatch ports of a reservation station; James S. Griffith, et al., 395/393, 390, 391, 672, 674, 675 [IMAGE AVAILABLE]
4. 5,666,505, Sep. 9, 1997, Heuristic prefetch mechanism and method for computer system; Joseph A. Bailey, 395/383; 364/263.1, 948, DIG.1, DIG.2 [IMAGE AVAILABLE]
5. 5,664,136, Sep. 2, 1997, High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations; David B. Witt, et al., 395/384, 376, 388, 391 [IMAGE AVAILABLE]
6. 5,659,782, Aug. 19, 1997, System and method for handling load and/or store operations in a superscalar microprocessor; Cheryl D. Senter, et al., 395/800.23; 364/DIG.1, DIG.2; 395/376, 800.41 [IMAGE AVAILABLE]
7. 5,655,098, Aug. 5, 1997, High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format; David B. Witt, et al., 395/386, 376, 380, 389, 586; 711/201 [IMAGE AVAILABLE]
8. 5,655,097, Aug. 5, 1997, High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format; David B. Witt, et al., 395/380, 376, 382, 386; 711/147 [IMAGE AVAILABLE]
9. 5,651,125, Jul. 22, 1997, High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations; David B. Witt, et al., 395/394, 306, 391, 393; 711/146 [IMAGE AVAILABLE]
10. 5,649,225, Jul. 15, 1997, Resynchronization of a superscalar processor; Scott A. White, et al., 395/800.23; 364/231.8, 948.34, DIG.1, DIG.2; 395/800.01 [IMAGE AVAILABLE]
11. 5,632,023, May 20, 1997, Superscalar microprocessor including flag operand renaming and forwarding apparatus; Scott A. White, et al., 395/394, 391, 800.23 [IMAGE AVAILABLE]
12. 5,630,157, May 13, 1997, Computer organization for multiple and out-of-order execution of condition code testing and setting instructions; Harry Dwyer, III, 395/800.23; 364/261.3, 261.5, DIG.1; 395/390 [IMAGE AVAILABLE]
13. 5,630,082, May 13, 1997, Apparatus and method for instruction queue scanning; Nathan L. Yao, et al., 395/389, 800.23 [IMAGE AVAILABLE]
14. 5,627,984, May 6, 1997, Apparatus and method for entry allocation for a

buffer resource utilizing an internal two cycle pipeline; Shantanu R. Gupta, et al., 395/376; 364/955.2, 958.2, DIG.2 [IMAGE AVAILABLE]

15. 5,615,402, Mar. 25, 1997, Unified write buffer having information identifying whether the address belongs to a first write operand or a second write operand having an extra wide latch; Marc A. Quattromani, et al., 395/800.38; 364/704, 749; 395/309, 566, 800.34; 711/200 [IMAGE AVAILABLE]

16. 5,613,132, Mar. 18, 1997, Integer and floating point register alias table within processor device; David W. Clift, et al., 395/393 [IMAGE AVAILABLE]

17. 5,606,676, Feb. 25, 1997, Branch prediction and resolution apparatus for a superscalar computer processor; Edward T. Grochowski, et al., 395/586, 386, 800.23 [IMAGE AVAILABLE]

18. 5,604,878, Feb. 18, 1997, Method and apparatus for avoiding writeback conflicts between execution units sharing a common writeback path; Robert P. Colwell, et al., 395/393; 364/231.8, 281.3, 281.8, 948.34, 964.26, DIG.1, DIG.2; 395/800.42, 826; 711/100 [IMAGE AVAILABLE]

19. 5,590,352, Dec. 31, 1996, Dependency checking and forwarding of variable width operands; Gerald D. Zuraski, Jr., et al., 395/800.23; 364/259.2, 263, 263.1, DIG.1 [IMAGE AVAILABLE]

20. 5,590,348, Dec. 31, 1996, Status predictor for combined shifter-rotate/merge unit; James E. Phillips, et al., 395/564; 364/DIG.2; 395/800.23 [IMAGE AVAILABLE]

21. 5,560,032, Sep. 24, 1996, High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution; Le Trong Nguyen, et al., 395/800.23; 364/931.11, 931.41, 931.55, DIG.2; 395/393, 394 [IMAGE AVAILABLE]

22. 5,560,025, Sep. 24, 1996, Entry allocation apparatus and method of same; Shantanu R. Gupta, et al., 395/800.23; 364/231.8, 239.4, 261, 262.4, 263.3, 280, DIG.1, DIG.2; 395/382, 393 [IMAGE AVAILABLE]

23. 5,557,763, Sep. 17, 1996, System for handling load and/or store operations in a superscalar microprocessor; Cheryl D. Senter, et al., 395/800.23; 364/DIG.1, DIG.2; 395/385; 711/140 [IMAGE AVAILABLE]

24. 5,553,256, Sep. 3, 1996, Apparatus for pipeline streamlining where resources are immediate or certainly retired; Michael A. Fetterman, et al., 395/393; 711/204 [IMAGE AVAILABLE]

25. 5,548,776, Aug. 20, 1996, N-wide bypass for data dependencies within register alias table; Robert P. Colwell, et al., 395/393; 364/238, 239, 246.3, DIG.1; 395/394, 800.23 [IMAGE AVAILABLE]

26. 5,539,911, Jul. 23, 1996, High-performance, superscalar-based computer system with out-of-order instruction execution; Le T. Nguyen, et al., 395/800.23 [IMAGE AVAILABLE]

27. 5,524,262, Jun. 4, 1996, Apparatus and method for renaming registers in a processor and resolving data dependencies thereof; Robert P. Colwell, et al., 395/800.23; 364/231.8, 247, 256.3, 262.4, DIG.1; 395/391, 393, 394 [IMAGE AVAILABLE]

28. 5,499,352, Mar. 12, 1996, Floating point register alias table FXCH and retirement floating point register array; David W. Clift, et al., 395/393; 364/DIG.1; 395/800.23; 711/202 [IMAGE AVAILABLE]
29. 5,499,204, Mar. 12, 1996, Memory cache with interlaced data and method of operation; David Barrera, et al., 365/49, 189.02, 230.01; 395/391; 711/100 [IMAGE AVAILABLE]
30. 5,490,280, Feb. 6, 1996, Apparatus and method for entry allocation for a resource buffer; Shantanu R. Gupta, et al., 395/800.23; 364/931.11, 931.41, 931.55, 939, DIG.2; 395/393 [IMAGE AVAILABLE]
31. 5,471,598, Nov. 28, 1995, Data dependency detection and handling in a microprocessor with write buffer; Marc A. Quattromani, et al., 711/122; 364/231.8, 243.4, 243.41, 964, 964.2, DIG.1, DIG.2; 395/394, 800.23 [IMAGE AVAILABLE]
32. 5,471,593, Nov. 28, 1995, Computer processor with an efficient means of executing many instructions simultaneously; Michael H. Branigin, 395/24 [IMAGE AVAILABLE]
33. 5,463,745, Oct. 31, 1995, Methods and apparatus for determining the next instruction pointer in an out-of-order execution computer system; Rohit A. Vidwans, et al., 395/394; 364/262.4, 946.2, DIG.1, DIG.2 [IMAGE AVAILABLE]
34. 5,446,912, Aug. 29, 1995, Partial width stalls within register alias table; Robert P. Colwell, et al., 395/393, 380, 800.23 [IMAGE AVAILABLE]
35. 5,442,756, Aug. 15, 1995, Branch prediction and resolution apparatus for a superscalar computer processor; Edward T. Grochowski, et al., 395/585; 364/231.8, 239.4, 261.7, DIG.1; 395/586, 587, 800.23 [IMAGE AVAILABLE]
36. 5,434,985, Jul. 18, 1995, Simultaneous prediction of multiple branches for superscalar processing; Philip G. Emma, et al., 395/587; 364/259.2, 261.3, 261.7, 262.4, 263.1, DIG.1; 395/391 [IMAGE AVAILABLE]
37. 5,416,913, May 16, 1995, Method and apparatus for dependency checking in a multi-pipelined microprocessor; Edward T. Grochowski, et al., 395/392; 364/230, 230.3, 262.4, 263, DIG.1; 395/800.23 [IMAGE AVAILABLE]
38. 5,151,981, Sep. 29, 1992, Instruction sampling instrumentation; Douglas W. Westcott, et al., 395/185.03; 364/229, 232.7, 232.9, 238.3, 239, 239.6, 243.4, 243.41, 261.3, 262.4, 262.9, 264, 265.6, 280, DIG.1; 395/184.01 [IMAGE AVAILABLE]

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